EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L2	1	("6534414").PN.	US-PGPUB; USPAT	OR	OFF	2006/06/01 13:57
L3	30	(dual adj mask) same (etching or removing)	US-PGPUB; USPAT	OR	ON	2006/06/01 14:16
L4	6	(dual adj mask) same (etching or removing)	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/01 14:25
L5	3873	438/283,287,290,299,301,303.ccls.	US-PGPUB; USPAT	OR	ON	2006/06/01 14:23
L6	3069	5 and (mask or photomask or resist or photoresist or (hard adj mask))	US-PGPUB; USPAT	OR	ON	2006/06/01 14:24
L7	2769	6 and @ad<"20040318"	US-PGPUB; USPAT	OR	ON	2006/06/01 14:29
L8	2745	7 and (gate or electrode)	US-PGPUB; USPAT	OR	ON	2006/06/01 14:24
L9	204589	"257"/$.ccls.	US-PGPUB; USPAT	OR	ON	2006/06/01 14:24
L10	106223	9 and (mask or photomask or resist or photoresist or (hard adj mask))	US-PGPUB; USPAT	OR	ON	2006/06/01 14:28
L11	80471	10 and (gate or electrode)	US-PGPUB; USPAT	OR	ON	2006/06/01 14:24
L12	77866	11 not 8	US-PGPUB; USPAT	OR	ON	2006/06/01 14:24
L13	66772	12 and (removing or etching)	US-PGPUB; USPAT	OR	ON	2006/06/01 14:25
L14	15012	13 and (self adj aligned)	US-PGPUB; USPAT	OR	ON	2006/06/01 14:26
L15	4316	14 and (second adj (region or area or portion or gate or stack))	US-PGPUB; USPAT	OR	ON	2006/06/01 14:27
L16	3428	15 and ((etch or etching or removing) with (mask or photomask or resist or photoresist or (hard adj mask)))	US-PGPUB; USPAT	OR	ON	2006/06/01 14:28
L17	3088	16 and @ad<"20040318"	US-PGPUB; USPAT	OR	ON	2006/06/01 14:45
L19	10648	((gate or electrode) and (dielectric or insulator or insulating or insulative) and (mask or photomask or resist or photoresist or (hard adj mask)) and (etch or etching or remove or removing)).clm. and @ad<"20040318"	US-PGPUB; USPAT	OR	ON	2006/06/01 14:46

EAST Search History

L21	1285	((gate or electrode) and (dielectric or insulator or insulating or insulative) and (mask or photomask or resist or photoresist or (hard adj mask)) and (etch or etching or remove or removing) and (second adj (region or area or portion))). clm. and @ad<"20040318"	US-PGPUB; USPAT	OR	ON	2006/06/01 14:47

DOCUMENT-IDENTIFIER: US 20040241919 A1

TITLE: Method of forming a CMOS thin film transistor device

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Abstract Paragraph - ABTX (1):

A method of forming a CMOS thin film transistor device. A dry **etching** procedure is performed to remove part of a **photoresist** layer and part of a metal layer and thus forms a **gate** with a symmetrical cone shape and a remaining **photoresist** layer. The dielectric layer is thus exposed in the lightly doped area. Specially, the bottom width of the first **gate** is narrower than that of the first metal layer and the symmetrical cone shape is gradually thinner from bottom to top. Using the **gate as a mask,** an n.sup.--ion implantation is performed to form a **self-aligned** and symmetrical LDD region in a semiconductor layer without additional photolithography steps.

Current US Classification, US Secondary Class/Subclass - CCSR (1):

257/E21.703

Current US Classification, US Secondary Class/Subclass - CCSR (2):

257/E27.111

Summary of Invention Paragraph - BSTX (7):

[0006] In FIG. 1A, a glass substrate 100 having an NMOS area 110 and a PMOS area 120 is provided. By performing a first patterning process using a first **photomask,** a first polysilicon island 130 and a second polysilicon island 135 are formed on the substrate 100. The first polysilicon island 130 is located in the NMOS area 110 and the second polysilicon island 135 is located in the PMOS area 120.

Summary of Invention Paragraph - BSTX (8):

[0007] In FIG. 1A, a silicon oxide (SiO.sub.x) layer 140 is formed over the polysilicon islands 130 and 135 and the substrate 100. A metal layer (not shown) is then formed on the silicon oxide layer 140. By performing a second patterning process using a second **photomask,** the metal layer (not shown) is patterned to form a first **gate** 141 and a **second gate** 142 on part of the silicon oxide layer 140. The first **gate** 141 is located in the NMOS area 110 and the

second gate 142 is located in the PMOS area 120.

Summary of Invention Paragraph - BSTX (9):
[0008] In FIG. 1B, using the first **gate** 141 and the **second gate** 142 as a **mask,** an n.sup.--ion implantation 150 is performed to form an n.sup.--polysilicon film 151 in part of the first polysilicon island 130 and part of the second polysilicon island 135. The n.sup.--polysilicon film 151 serves as an LDD (lightly doped drain) structure 151.

Summary of Invention Paragraph - BSTX (10):
[0009] In FIG. 1C, by performing a third patterning process using a third **photomask,** a first **photoresist** pattern 160 is formed to cover the PMOS area 120 and part of the NMOS area 110. Then, an n.sup.+-ion implantation 170 is performed to form an n.sup.+-polysilicon film 171 in part of the first polysilicon island 130. The n.sup.+-polysilicon film 171 serves as a source/drain region. Thus, an NMOS TFT 175 is obtained. It should be noted that, referring to FIG. 1E, misalignment occurs easily in the NMOS area 110 due to use of multiple **photomasks,** specifically due to the use of a second **photomask** which is different from the third **photomask**. This causes the LDD structure 151 (or n.sup.+-polysilicon film) to be narrower on one side and wider on the other side. That is, the LDD structure 151 (or n.sup.--polysilicon film) is not symmetrically located in the first polysilicon layer 130 beside the first **gate** 141, thereby increasing leakage current.

Summary of Invention Paragraph - BSTX (11):
[0010] In FIG. 1D, the first **photoresist** pattern 160 is removed. By performing a fourth patterning process using a fourth **photomask,** a second **photoresist** pattern 180 is formed to cover the NMOS area 110. Then, a p.sup.+-ion implantation 190 is performed to form a p.sup.+-polysilicon film 191 in part of the second polysilicon island 135. The p+-polysilicon film 191 serves as a source/drain region. Thus, a PMOS TFT 195 is obtained. Lastly, the second **photoresist** pattern 180 is removed, as shown as FIG. 1E.

Summary of Invention Paragraph - BSTX (12):
[0011] The conventional method uses two different **photomasks** to define the **gate** and the LDD structure, often resulting in misalignment. This causes an asymmetrical LDD structure in the NMOS TFT, thereby increasing leakage current. In addition, the conventional method requires four **photomasks,** which is complicated and expensive.

Summary of Invention Paragraph - BSTX (14):
[0012] One object of the present invention is to provide a method of forming

a CMOS TFT device having a **self-aligned** and symmetrical LDD structure.

Summary of Invention Paragraph - BSTX (16):

[0014] In order to achieve these objects, the present invention provides a method of forming a CMOS thin film transistor device. A substrate having an NMOS area, a PMOS area and a circuit area is provided, wherein the NMOS area further comprises a first doped area, a lightly doped area and a first **gate** area, and the PMOS area further comprises a second doped area and a **second gate** area. By performing a first patterning process using a first **photomask,** a first semiconductor island and a second semiconductor island are formed on part of the substrate, wherein the first semiconductor island is located in the NMOS area and the second semiconductor island is located in the PMOS area. A dielectric layer is formed on the first semiconductor island, the second semiconductor island and the substrate. A metal layer is formed on the dielectric layer. By performing a second patterning process using a second **photomask,** a first **photoresist** layer is formed on the metal layer located in the lightly doped area, the first **gate** area, the PMOS area and the circuit area. Using the first **photoresist** layer as a **mask,** part of the metal layer is removed to form a first metal layer in the lightly doped area and the first **gate** area, a second metal layer in the PMOS area and a third metal layer in the circuit area, wherein the third metal layer electrically connects the first metal layer and the second metal layer. Using the first and second metal layers as **masks,** an n.sup.+-ion implantation is performed to form a first source/drain region in the first semiconductor island in the first doped area. By performing a dry **etching** procedure, part of the first **photoresist** layer, part of the first metal layer and part of the second metal layer are removed to form a first **gate** with a symmetrical cone shape, a remaining second metal layer and a remaining first **photoresist** layer, thereby exposing the dielectric layer in the lightly doped area. Specially, a bottom width of the first **gate** is narrower than that of the first metal layer and the symmetrically coned shape is gradually thinner from bottom to top. Using the first **gate** and the remaining second metal layer as **masks,** an n.sup.--ion implantation is performed to form an LDD (lightly doped drain) region in the first semiconductor layer in the lightly doped area. The remaining first **photoresist** layer is removed and thus an NMOS element is formed in the NMOS area. By performing a third patterning process using a third **photomask,** the remaining second metal layer in the second doped area is removed to form a **second gate** on the dielectric layer in the **second gate** area. A p.sup.+-ion implantation is performed to form a second source/drain region in the second semiconductor island in the second doped area and thus a PMOS element is formed in the PMOS area.

Summary of Invention Paragraph - BSTX (17):

[0015] The present invention improves on the prior art in that part of the first metal layer and part of the second metal layer are removed to form a first **gate** with a symmetrical cone shape and a remaining second metal layer, thereby exposing the dielectric layer in the lightly doped area. Specially, the bottom width of the first **gate** is narrower than that of the first metal layer and the symmetrically coned shape is gradually thinner from bottom to top. Using the first **gate** and the remaining second metal layer as **masks,** an n.sup.--ion implantation is performed to form a **self-aligned** and symmetrical LDD region in the first semiconductor layer in the lightly doped area. Thus, the present invention requires only three **photomasks** to form the CMOS TFT with LDD structure, thereby decreasing costs and ameliorating the disadvantages of the prior art.

Detail Description Paragraph - DETX (3):

[0021] In FIGS. 2A and 2B, a substrate 200 having a predetermined NMOS area 210, a predetermined PMOS area 220 and a predetermined circuit area 230 is provided. The substrate 200 can be a glass or quartz substrate. The NMOS area 210 further comprises a first doped area 211, a lightly doped area 212 and a first **gate** area 213. The PMOS area 220 further comprises a second doped area 221 and a **second gate** area 222.

Detail Description Paragraph - DETX (4):

[0022] In FIGS. 2A and 2B, a semiconductor layer (not shown) is formed. By performing a first patterning process using a first **photomask** (or reticle) on the semiconductor layer (not shown), a first semiconductor island 240 and a second semiconductor island 245 are then formed on part of the substrate 200. The first semiconductor island 240 and the second semiconductor island 245 can be polysilicon layers. The first semiconductor island 240 is located in the NMOS area 210 and the second semiconductor island 245 is located in the PMOS area 220. Then, a dielectric layer 250, such as silicon oxide (SiO.sub.x) or silicon nitride (SiN.sub.x), is formed on the first semiconductor island 240, the second semiconductor island 245 and the substrate 200. The dielectric layer 250 serves as a **gate** insulating layer.

Detail Description Paragraph - DETX (5):

[0023] In FIGS. 2A and 2B, a metal layer 260 is formed on the dielectric layer 250. The metal layer 260 can be a molybdenum (Mo) layer. By performing a second patterning process using a second **photomask,** a first **photoresist** layer 270 is formed on the metal layer 260 located in the lightly doped area 212, the first **gate** area 213, the PMOS area 220 and the circuit area 230.

Detail Description Paragraph - DETX (6):

[0024] In FIGS. 3A and 3B, using the first **photoresist** layer 270 as a **mask,** part of the metal layer 260 is removed to form a first metal layer 261 in the lightly doped area 212 and the first **gate** area 213, a second metal layer 262 in the PMOS area 220 and a third metal layer 263 in the circuit area 230. The method of **removing** part of the metal layer 260 can be dry or wet **etching,** preferably, Cl.sub.2 is used as an **etching** gas for dry **etching**. The third metal layer 263 electrically connects the first metal layer 261 and the second metal layer 262, as shown as FIG. 3A. In FIG. 3A, the first **photoresist** layer 270 is not shown.

Detail Description Paragraph - DETX (7):

[0025] In FIGS. 4A and 4B, using the first metal layer 261 and the second metal layer 262 as **masks,** an n.sup.+-ion implantation 280 is performed to form a first source/drain region 281, such as an n.sup.+-polysilicon film, in the first semiconductor island 240 in the first doped area 211. The n.sup.+-ions of the implantation 280 can be P.sup.+ or As.sup.+ ions. For example, the dose of the n.sup.+-ions is about 1E15 atom/cm.sup.2. In FIG. 4A, the first **photoresist** layer 270 is not shown.

Detail Description Paragraph - DETX (8):

[0026] In FIGS. 5A and 5B, a dry **etching** procedure is performed to uniformly remove part of the first **photoresist** layer 270, part of the first metal layer 261 and part of the second metal layer 262, thereby forming a first **gate** 290 with a symmetrical cone shape in the first **gate** area 213, a remaining second metal layer 262' in the PMOS area 220 and a remaining first **photoresist** layer 270' in the PMOS area 220 and exposing the dielectric layer 250 in the lightly doped area 212. It should be noted that the bottom width of the first **gate** 290 is narrower than that of the first metal layer 261, and the symmetrically coned shape is gradually thinner from bottom to top. For example, an included angle .theta. at the bottom of the symmetrically coned shape (290) is less than 45.degree., as shown in FIG. 5B. In this embodiment, the **etching** gas of the dry **etching** procedure can be Cl.sub.2 and O.sub.2, wherein an **etching** selectivity of the first **photoresist** layer 270' to the metal layer 260 (e.g. Mo layer) ranges from 1 to 1/4.

Detail Description Paragraph - DETX (9):

[0027] In FIGS. 6A and 6B, using the first **gate** 290 and the remaining second metal layer 262' as **masks,** an n.sup.--ion implantation 300 is performed to form a **self-aligned** LDD (lightly doped drain) region 310 in the first semiconductor layer 240 in the lightly doped area 212. The n.sup.--ions of the implantation 300 can be P.sup.+ or As.sup.+ ions. For example, the dose of the n.sup.--ions is about 1E13 atom/cm.sup.2.

Detail Description Paragraph - DETX (10):

[0028] It should be noted that, referring to FIG. 6B, the two sides of the first **gate** 290 have a symmetrical slope due to the above-mentioned uniform dry **etching**. Thus, the present method can easily form a **self-aligned** and symmetrical LDD region 310 in the first semiconductor island 240 located below the two sides of the first **gate** 290.

Detail Description Paragraph - DETX (11):

[0029] In FIGS. 7A and 7B, the remaining first **photoresist** layer 270' is then removed. Thus, an NMOS element 320 is obtained in the NMOS area 210.

Detail Description Paragraph - DETX (12):

[0030] Next, referring to FIGS. 8A and 8B, by performing the third patterning process using the third **photomask,** a second **photoresist** layer 330 is formed to cover the NMOS area 221, the circuit area 230 and the **second gate** area 222. That is, the second **photoresist** layer 330 only exposes the second doped area 221. In order to thoroughly remove the remaining second metal layer 262' in the second doped area 221, both sides of the remaining second metal layer 262' should be exposed in an opening of the second **photoresist** layer 330.

Detail Description Paragraph - DETX (13):

[0031] In FIGS. 9A and 9B, using the second **photoresist** layer 330 as a **mask,** the remaining second metal layer 262' in the second doped area 221 is removed to form a **second gate** 340 on the dielectric layer 250 in the **second gate** area 222. The method of **removing** the remaining second metal layer 262' can be wet or dry **etching**. Preferably dry **etching** is performed with Cl.sub.2 as the **etching** gas.

Detail Description Paragraph - DETX (14):

[0032] In FIGS. 10A and 10B, using the second **photoresist** layer 330 and the **second gate** 340 as **masks,** the p.sup.+-ion implantation 350 is performed to form the second source/drain region 351 in the second semiconductor island 245 in the second doped area 221. Thus, a PMOS element 360 is obtained in the PMOS area. The p.sup.+-ions of the implantation 350 can be B.sup.+ ions.

Detail Description Paragraph - DETX (15):

[0033] Lastly, referring to FIGS. 11A and 11B, the second **photoresist** layer 330 is removed. Thus, a CMOS TFT device comprising the NMOS element 320 and the PMOS element 360 is obtained.

Detail Description Paragraph - DETX (16):

[0034] The present invention provides a method of forming a CMOS TFT device with an LDD structure. The present method uses only three photolithography steps to form the CMOS TFT device. A feature of the method is that the first metal layer is removed to form a first **gate** with a symmetrical cone shape, thereby exposing the dielectric layer in the lightly doped area. Specifically, the bottom width of the first **gate** is narrower than that of the first metal layer and the symmetrically coned shape is gradually thinner from bottom to top. Using the first **gate** and the remaining second metal layer as **masks,** an n.sup.--ion implantation is performed to form a **self-aligned** and symmetrical LDD region in the first semiconductor layer without additional photolithography steps. Thus, the present invention requires only three **photomasks** to fabricate the CMOS TFT with symmetrical LDD structure, thereby reducing leakage current and manufacturing cost and ameliorating the disadvantages of the prior art.

Claims Text - CLTX (2):

1. A method of forming a CMOS thin film transistor device on a substrate having an NMOS area, a PMOS area and a circuit area, the NMOS area having a first doped area, a lightly doped area and a first **gate** area, and the PMOS area having a second doped area and a **second gate** area, the method comprising the steps of: (a) forming a semiconductor layer on the substrate; (b) performing a first patterning process using a first **photomask** on the semiconductor layer to form a first semiconductor island and a second semiconductor island on part of the substrate, wherein the first semiconductor island is located in the NMOS area and the second semiconductor island is located in the PMOS area; (c) forming a dielectric layer on the first semiconductor island, the second semiconductor island and the substrate; (d) forming a metal layer on the dielectric layer; (e) performing a second patterning process using a second **photomask** to form a first **photoresist** layer on the metal layer located in the lightly doped area, the first **gate** area, the PMOS area and the circuit area; (f) using the first **photoresist** layer as a **mask, removing** part of the metal layer to form a first metal layer in the lightly doped area and the first **gate** area, a second metal layer in the PMOS area and a third metal layer in the circuit area, wherein the third metal layer electrically connects the first metal layer and the second metal layer; (g) using the first and the second metal layers as **masks,** performing an n.sup.+-ion implantation to form a first source/drain region in the first semiconductor island in the first doped area; (h) performing a dry **etching** procedure to remove part of the first **photoresist** layer, part of the first metal layer and part of the second metal layer, thus forming a first **gate** with a symmetrical cone shape, a remaining second metal layer and a remaining first **photoresist** layer, and exposing the dielectric layer in the lightly doped area, wherein a bottom width of the first **gate** is narrower than that of the first metal layer, and the symmetrically coned shape